

## A Proposed 68HC11 Chip Set for 275 degrees C

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### Abstract

*The 68HC11 microprocessor is widely used in well logging tools for control, data acquisition, and signal processing applications. This high temperature version of the 68HC11 enables new high temperature designs and additionally allows 68HC11-based well logging tools and MWD tools to be upgraded for high temperature operation in deep gas reservoirs. In this project, funded by the U. S. Department of Energy, we will design and construct a chip set for 275 °C operation that consists of a 68HC11 single chip microcomputer and two serial peripheral memory chips. The microcomputer chip consists of the microprocessor ALU, a small boot ROM, 8 kbyte data RAM, counter/timer unit, serial peripheral interface (SPI), asynchronous serial interface (SCI), and the A, B, C, and D parallel ports. The chip will be pin and binary code compatible with the single chip mode commercial 68HC11 except for the absence of the analog to digital converter system. To avoid mask programmed internal ROM, a boot program is used to load the microcomputer program from an external mask ROM serial peripheral chip. A RAM serial peripheral chip completes the chip set and allows data RAM to be added in 8 kbyte increments. The system will be implemented in the Peregrine Semiconductor 0.5 micron Silicon-on-Sapphire (SOS) process using a custom high temperature cell library developed at Oklahoma State University. As much as possible, this cell library will be used with public-domain Verilog code for the 68HC11 for rapid compilation and simulation testing of the chip set before fabrication at the foundry. We intend to apply the lessons learned in this project to development of high temperature versions of other microcomputer workhorses, such as the PIC or ARM microcomputer chips.*

Keywords: 68HC11, high temperature electronics, embedded systems, silicon-on-insulator, SOI

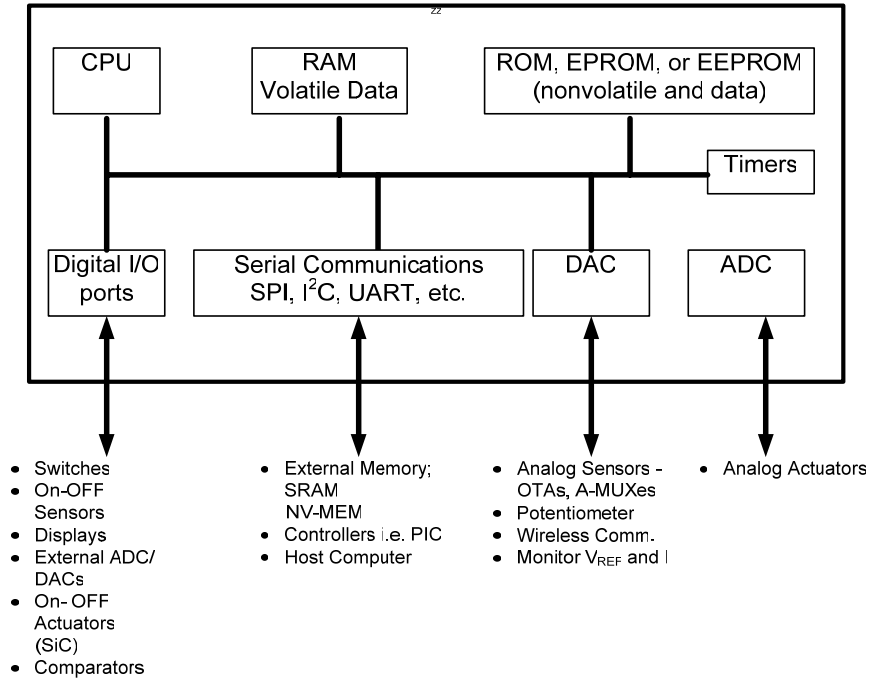
### 1.0 Introduction

This paper describes a project for the design, construction and testing of a 68HC11 microprocessor chip set that will operate at 275 °C. The chip set is being implemented in the Peregrine UltraCMOS 0.5 micron silicon-on-sapphire (SOS) process [1]. The chip set is intended for well logging applications in very deep and hot wells and is being funded by the U. S. Department of Energy as part of their Deep Trek program [2].

Given the increasing demand for energy world-wide, there has been growing pressure to explore for oil and gas at ever deeper subsurface depths as shallow reservoirs are depleted. As result, there is an increasing need for electronics that can operate at the extreme temperatures associated with drilling and production of deep reservoirs. In oil and gas exploration and production, electronic circuits are used for control and steering of the bit during drilling, for measurement while drilling (MWD), for well logging, and in situ production management. Among these electronic functions, microcontroller circuits are important for control, communications, data

acquisition, and simple digital signal processing.

As shown in Figure 1, microcontrollers are self contained single-chip computers with all necessary processing and I/O functions included on-chip: 1) read-only memory (ROM), 2) random access memory (RAM), 3) parallel I/O, 4) asynchronous serial I/O, 5) synchronous serial I/O, 6) counter/timer system, 7) analog to digital converter (ADC), and 8) digital to analog converts (DAC). Microcontrollers are available in roughly three ranges of complexity, depending on their speed and processing capability. See Table 1. Low-end microcontrollers, such as the PIC [3] are simple devices with very low pin count (down to 8 pins) and are capable of executing simple control programs. Mid-range microcontrollers, such as the 68HC11 [4], are fairly complex devices, that can have high pin counts, up to 100 pins. These microcontrollers can be used for complex control functions and usually possess arithmetic capability suitable for simple digital signal processing (DSP) applications. High-end microcontrollers, represented by the ARM processor [5], are complex devices with high pin



**Figure 1. Diagram of a typical microcontroller circuit.**

counts that are fast and complex high performance pipelined devices with math coprocessors for sophisticated control algorithms and complex, high speed DSP.

For MWD and well logging applications, the 68HC11 represents a good general purpose microcontroller that is suitable for many modest applications. Furthermore, the 68HC11 has been in existence since the mid-1980's and has been widely used in the oil and gas industry. A great number of existing MWD tools and well logging tools use the 68HC11. The 275 °C version of the 68HC11 being developed will provide a relatively easy migration path to high temperature versions for these existing systems.

The original 68HC11 was implemented in bulk CMOS, technologies that are currently in wide

use. Bulk CMOS is typically not suitable for extreme temperature applications because of the leakage currents associated with well isolation junctions and the transistor drain to body diodes. These currents tend to increase catastrophically above 125 °C. Silicon-on-insulator (SOI) processes have thinner bodies and isolated transistor bodies, situated as "islands" on an insulating substrate. As a result leakage currents in SOI processes are very low, allowing SOI digital circuits to function to as high as 300 °C [6]. Figure 2a shows the off state leakage currents for a Peregrine SOS NMOS transistor at 30 and 195 °C. Figure 2b shows the transfer characteristic of a 3 input CMOS NAND gate at 225 °C, illustrating its stability even at high temperatures.

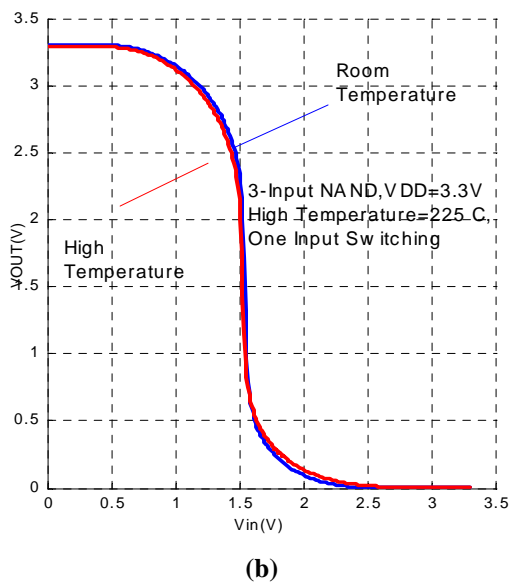
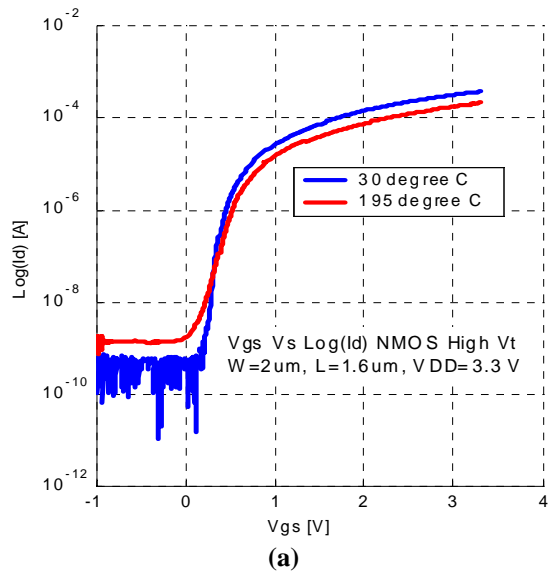
**Table 1. Comparison of low-end, medium-range, and high-end microprocessor capabilities.**

Processor	Example	Capabilities	Applications
Low-end	PIC	8 bit data acquisition and control NO co-preprocessor	Simple instrument control, and high volume consumer products
Mid-range	68HC11, 8051	16 bit data acquisition and control and low end DSP. Enhanced math functions or co-processor	General purpose instrument control and light signal processing
High-end	ARM	> 16 bit data acquisition & control & high end DSP. Specialized math operations.	Complex controls and digital signal processing, and high performance, low volume military/consumer products

The 68HC11 will be implemented using Peregrine Semiconductor's 0.5 micron UltraCMOS silicon-on-sapphire (SOS) process [1], a commercially available SOI process that features fully depleted dielectrically isolated devices. Transistors in this process are implemented with low, high, and medium threshold voltages. For digital circuits, high level threshold voltages are used to minimize off state leakage.

## 2.0 Design Goals

Figure 3 shows a block diagram for a downhole microcomputer system based on the



**Figure 2. (a) Typical leakage currents in SOI devices, (b) Extreme temperature transfer characteristics of CMOS SOI inverter.**

proposed 275 °C 68HC11 microcomputer chip set. This system consists of the 68HC11 IC, local peripheral devices, and remote devices. The 68HC11 consists of: 1) a microprocessor core, and its associated boot ROM and program RAM and, 2) internal peripherals including a timer system, parallel I/O, and a serial peripheral interface (SPI) circuit. The SPI is an industry standard high speed synchronous serial bus designed for short-range communications between digital devices. The 68HC11 can access several external peripheral devices through the SPI bus: 1) a masked program ROM, 2) external data RAM, 3) analog to digital converters (ADC), 4) digital to analog converters (DAC), 5) comparators, 6) long-range communication devices such as asynchronous serial devices (UARTs) or Manchester encoder/decoders, and 7) SPI-equipped instrumentation such as the quartz pressure transducer (QPT) device shown in the figure. In this system long range communications (between electronic subassemblies in the tool) is accomplished using either the asynchronous communication through a SPI/UART interface or a serial Manchester encoders/decoder IC. Remote devices and microcontrollers can communicate directly through the asynchronous link, or through a remote SPI/UART interface. Noise resistant asynchronous standards can be used, such as RS-485. Other long range serial communication standards can be implemented, such as Manchester encoding, LIN bus, or CAN bus. Serial Manchester encoders/decoders are currently under consideration as the long haul communications method of choice. The system outlined in Figure 3 is a highly adaptable, general purpose system that can be used to control all but the most demanding requirements for MWD and well logging instruments.

The proposed system is intended to be compatible with the 68HC11E, a general-purpose version of the 68HC11 family:

- The system will be able to operate for extended periods at an ambient temperature of 275 °C.
- Object code software compatibility has been maintained except for the SWI (software interrupt) instruction.
- Output drive strength is compatible with original 68HC11E specifications.

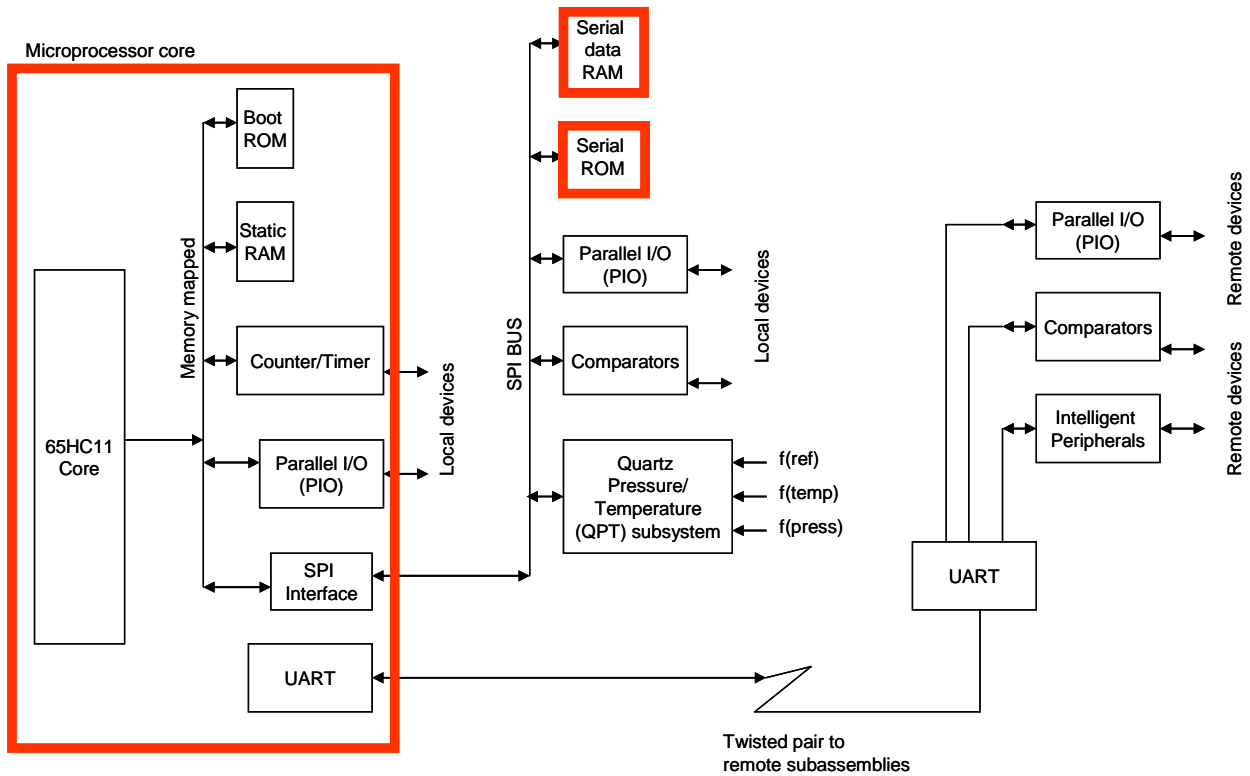


Figure 3. System block diagram for the proposed 68HC11-based 275 °C downhole microcomputer system.

- Because of the lack of availability of external peripheral devices, and the availability of a great number of 68HC11 software and hardware development systems, we will not implement the expanded mode of operation. This mode, generally used for expanding the 68HC11 for use in development systems, brings out the internal data and address busses of the 68HC11.
- Because of the lack of a reliable high temperature voltage reference and to restrict the scope of the project, we will not implement an on-chip analog to digital converter at this time. For the same reason, we do not implement analog comparator functions on this device.
- Because of the lack of reliable extreme temperature non-volatile memory, we do not implement programmable read only memory in this device. A small masked ROM is included which will contain a boot program for loading a program off the external SPI ROM through the SPI port. This program will be loaded into and run from the 68HC11 internal RAM.

### 3.0 68HC11 DMS Specifications

The 275 °C 68HC11 will function with a 3.3 volt supply voltage, and will have an 8 MHz maximum oscillator frequency, which results in a 2 MHz instruction cycle time (E clock rate). The

parallel outputs are designed for a maximum source current of 0.5 mA, and maximum sink current of 1 mA, for CMOS output logic levels of  $V_{OH} = 2.5$  volt and  $V_{OL} = 0.4$  volt.

Figure 4 shows a diagram of the programming model of the 68HC11. The processor uses two 8 bit accumulators, A and B, which can be concatenated into a 16 bit accumulator D. Two index registers are available, IX and IY, and a stack pointer, SP, program counter PC, and condition code register

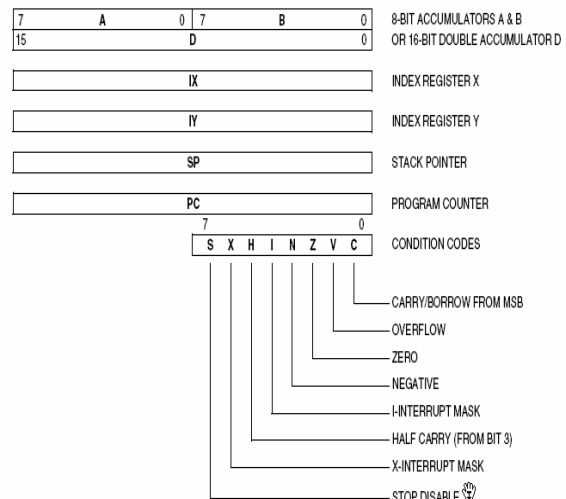
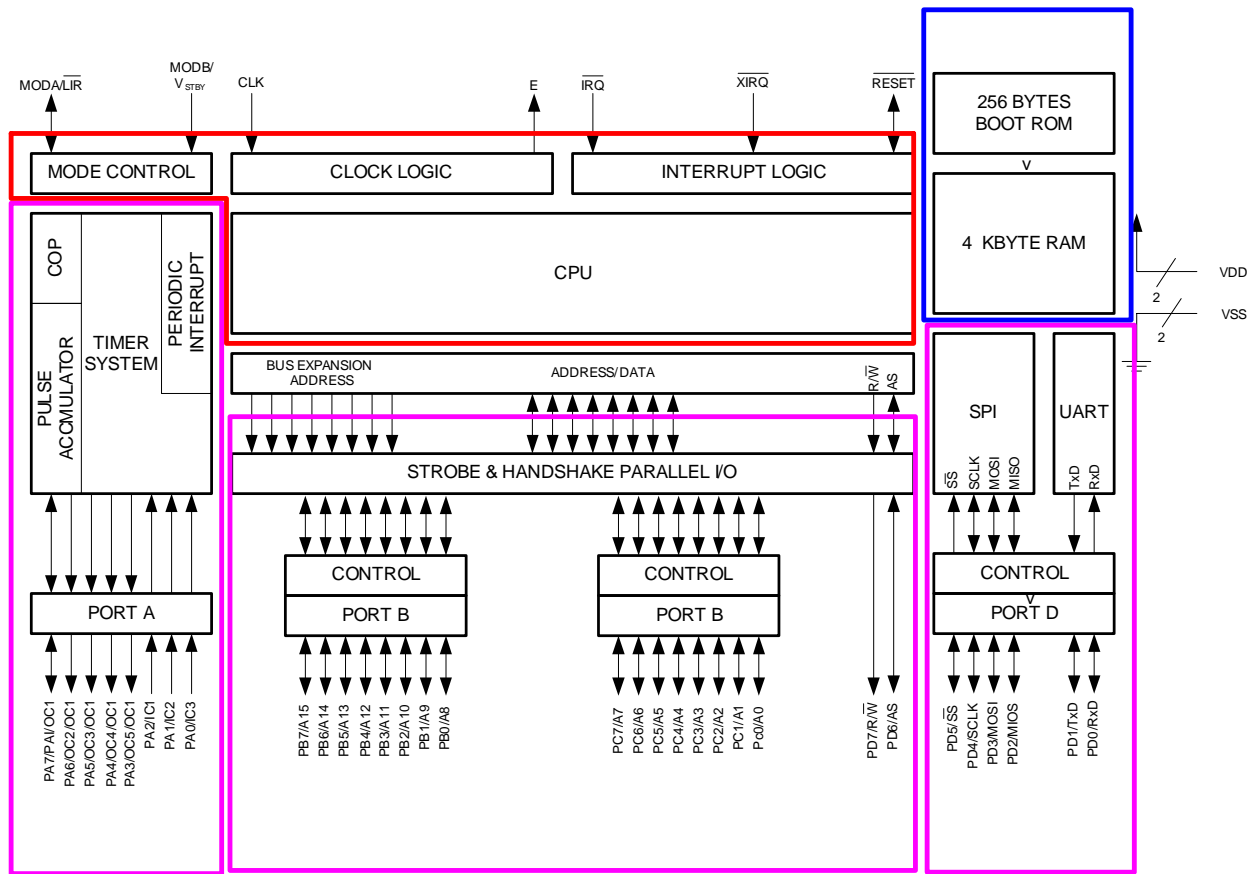


Figure 4. Programming model of the 68HC11.



**Figure 5. Diagram of the 275 °C 68HC11 showing functional blocks as implemented.**

CCR are also implemented. The processor is a standard Princeton or Von Neumann architecture with combined program and data storage and memory mapped I/O. This contrasts with the commonly used Harvard architecture (seen in PIC microcontrollers) where program storage and data memory are separated and port-based I/O is used. The instruction set is fairly large (>200 separate mnemonics) and uses five different addressing modes: Immediate, Direct, Extended, Indexed, Inherent, and Relative [4].

Figure 5 shows a diagram of the 275 °C 68HC11 as it will be implemented:

- The microcontroller core consists of an arithmetic logic unit (ALU), clock circuit, interrupt circuitry and mode control functions.
- The masked boot ROM will be used to control the 68HC11 immediately after reset, downloading the main program into RAM from external ROM through the SPI port. The 4 k-byte internal RAM serves as both program memory and internal data memory. Additional RAM memory can be accessed from an external RAM through the SPI port.
- The timer system consists of a free running 16

bit counter with a programmable 4 bit prescaler counter, all driven by the 2 MHz system clock. Three separate 16 bit input capture registers are available to capture timing of external events, and four separate output compare registers are available for generation of waveforms. An 8 bit pulse accumulator and gated timer is also implemented, as well as a computer operating properly (COP) timer.

- A serial peripheral interface (SPI) unit is implemented that can operate at a maximum bit clock rate of 2 MHz. The unit can operate in SPI master or slave mode.
- A universal asynchronous receiver transmitter (UART) is implemented that can be used for asynchronous serial communication.
- Parallel I/O is implemented as four 8 bit ports. Port A and Port D are shared with the timer system and the serial communication systems (SPI and UART) respectively. Port B is an output only port with a pulsed handshake mode. Port C is a bi-direction port that can be used with fully interlocked handshake with the STRB and STRA pins.
- An external masked ROM (not shown in Figure

5) is implemented to hold 4 k-byte of program memory to be booted into internal RAM. This ROM consists of a SPI interface circuit and 4 k-byte ROM.

- An external RAM (not shown in Figure 5) is implemented to hold 4 k-byte of data memory. This ROM consists of a SPI interface circuit and 4 k-byte RAM.

#### 4.0 Implementation Notes

A description of the cell library used in this project can be found in Badam, *et al* [7]. The OSU extreme temperature SOS standard cell library consists of 93 cells that are laid out on a pitch of 55 um. Individual transistors are laid out with gates that are about twice as long as minimum geometry devices. This is done to reduce high temperature leakage currents, which extends the maximum operating temperature of the process. As a general rule, the cells maximize the use of NANDs to decrease delay and minimize the use of NORs to reduce leakage currents. PMOS transistors in the Peregrine process have a lower off state leakage current than the NMOS transistors. NAND gates put these low leakage PMOS transistors in parallel and the NMOS devices in series, minimizing gate leakage

currents.

The HC11 circuit blocks will be implemented using the hardware description language Verilog HDL. A hardware synthesis program is used to implement the Verilog description of the circuit into a hardware integrated circuit layout using a standard cell library. We will use Cadence Tools, a well-known electronics computer-aided design (CAD) program, for hardware synthesis of integrated circuit layout of the 275 °C 68HC11 from Verilog source files using OSU's extreme temperature standard cell library.

In digital integrated circuit design, verification of proper design is critical, and takes up more than 75% of the time and labor in the design process. In this project we pursue a top-down design approach, breaking the design of the 68HC11 into *macrocells*, which are distinct functional blocks such as the timer system, or arithmetic logic unit. Verification is done by careful cross-checking of the functional specification of each macrocell against Verilog-based simulation test benches.

Testing of hardware will be accomplished in two stages: 1) on-wafer testing on an 8" Cascade Alessi REI-6100 semi automatic probe station, and 2) test of diced and mounted parts in a high temperature

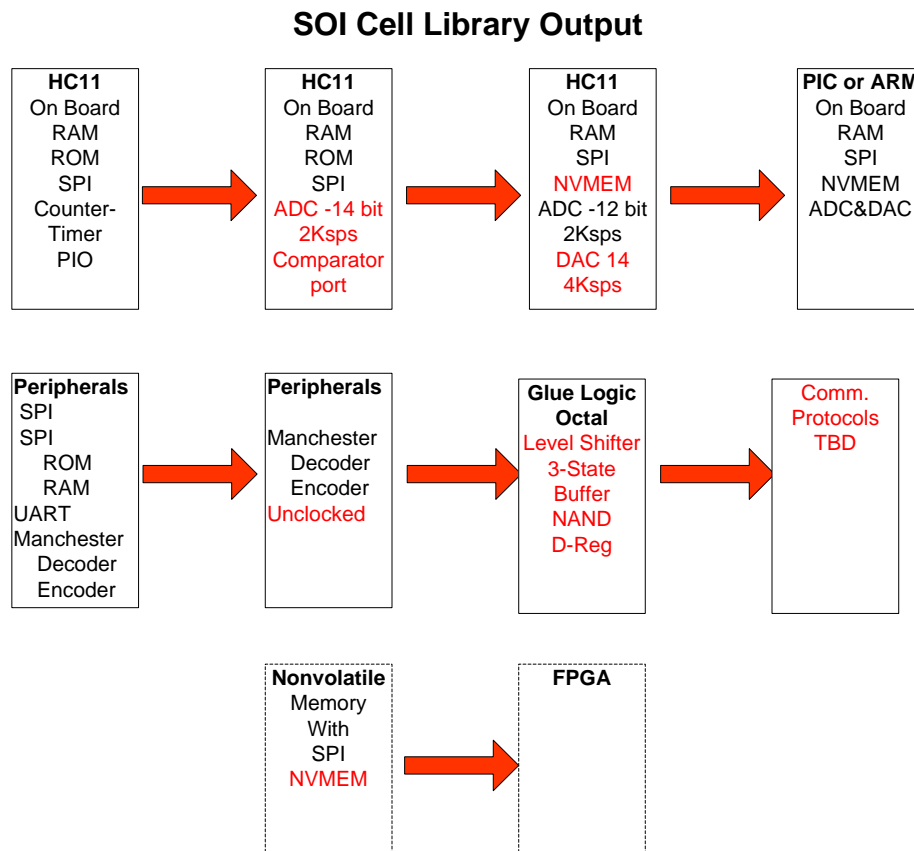


Figure 6. A proposed roadmap for extreme temperature instrumentation processors.

oven. OSU has acquired a 300 °C hot chuck for the probe station for wafer testing, and, we have developed in-house techniques of constructing and maintaining high temperature probe cards. When preparing test programs for wafer testing, FPGA (field programmable logic array) implementations of each macrocell will be used to fully debug test programs. This should minimize the time taken up on the wafer probe stations.

## 5.0 Perspective On An Extreme Temperature Electronics Roadmap

Figure 6 shows an informal roadmap for development of extreme temperature processor electronics for instrumentation. In our opinion it is important to implement technologically practical high temperature parts up front, in order to put electronic solutions in the hands of engineers as soon as possible. At the present time the most severe technological barrier for digital electronics is the lack of a programmable non-volatile memory circuit. This is preventing the development of both EEPROM memories and FPGAs for extreme temperature environments. A technological barrier for analog parts is the lack of a stable extreme temperature voltage reference, and the also the lack extreme temperature operational amplifiers.

Our proposed design is intended to step around these technological barriers in two ways: 1) we do not attempt to implement internal program memory in the 275 °C 68HC11, but design the device for use with external masked boot ROM. It is anticipated that programmable ROMs will be developed for use at progressively higher temperatures. The 68HC11 can be easily used with these devices in situations where the temperature doesn't exceed their capability. When a 275 °C programmable ROM becomes available, the 68HC11 can be redesigned to incorporate internal programmable ROM.

This philosophy also works for analog to digital (ADC) and digital to analog (DAC) circuits. As voltage references and operational amplifiers are developed to work at progressively higher temperatures, the 68HC11 can be used with these devices in environments that don't exceed their capabilities. It is merely necessary to design the ADC and DAC circuits with a SPI interface so that the 68HC11 can communicate with them.

## 6.0 Conclusion

We have presented a 275 °C 68HC11 microcontroller chip set that will be useful for well logging, MWD, and other extreme temperature environments. This device will answer a need for extreme temperature controller devices that can be

used for deep drilling. The project has an 18 month duration with final delivery of prototype parts expected in March of 2007. We have submitted layouts for macrocell test circuits to the foundry and expect delivery of the first wafers in late May 2006.

## 7.0 Acknowledgements

This Oklahoma State University project is funded by the U. S. Department of Energy, Contract No. DE-FC26-05NT42656.

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