

Design of a High Temperature Switched-Mode Power Supply Employing a V^2 Control Mechanism

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Abstract

The design of a switched-mode power supply (SMPS) employing V^2 control architecture for operation in excess of 225°C has been explored. The objective of the study is to prove the feasibility of a high-temperature SMPS and to determine the design metrics on the individual components to insure system stability over 25°C to 225°C. The study details the working of the V^2 control architecture with reference to a step-down switched-mode power supply and aims at providing performance specifications for individual blocks in the feedback design that would insure the feasibility of this design up to 225 °C.

The working of the V^2 control architecture is studied and relevant design equations are identified. A SPICE model for a switched-mode power supply using the V^2 control architecture has been developed which models the individual blocks of the V^2 feedback system. The model includes a soft-start mechanism, an over-current protection mechanism, an under-voltage lockout mechanism and a 100% duty cycle comparator.

The model was tested for a given set of input specifications at 25 °C and then the feasibility of this design was examined for a temperature range extending to 225 °C. Critical component parameters, varied to mimic anticipated temperature variation, have been included in the discussion. An example design and simulation describes a 25V dc input to a 5V output switched-mode power supply with better than 5% output dc regulation with excellent transient response with key components varied over greater than a $\pm 50\%$. The results of this study identifies challenges to extreme temperature power supply design and introduce a detailed algorithm for the design of V^2 switch mode (SM) power supplies.

Key words: extreme temperature SOI CMOS, V^2 controller, buck converter

1.0 Introduction

This paper describes a feasibility study of a high-temperature step-down switched-mode power supply employing V^2 control architecture [1]. The objective of this study is to show feasibility of an extreme temperature switched-mode power supply and determine the design metrics on the individual components that insure stability over temperature from 25 °C to 225 °C. The study details the operation of the V^2 control scheme when used with a step-down switched-mode power supply and determines performance specifications for the power supply individual functional blocks. From this we derive detailed specifications for a V^2 controller IC. Finally, we present a design algorithm for the V^2 architecture, along with SPICE simulation results.

The V^2 control architecture is a good voltage regulation scheme because it is robust over temperature and produces fast transient response to variations in load and line conditions. Consider that complex computer circuits, such as the Pentium IV, operate at low voltage, and pull enormous current spikes from their supply rails. At the GHz clock rates at which processors are ramped up and down to save power, changes in computational load to the processor causes massive transient changes in the current drawn by the processor. It is therefore extremely important that DC power supplies have exceptionally fast and robust response to transient load variations. Literature shows the V^2 control architecture to have faster transient characteristics when compared to the voltage mode and current mode control topologies [1-4]. This makes the V^2

control architecture a good choice for an extreme temperature SM (switched mode) power supply and SM power supply controller IC.

$$G_d(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{V_O}{D} \left[\frac{1 + sCR_C}{1 + s \left[\frac{L}{R + R_{ON} + R_L} + \frac{CR(R_{ON} + R_L)}{R + R_{ON} + R_L} + CR_C \right] + s^2 LC \left[\frac{R + R_C}{R + R_{ON} + R_L} \right]} \right] \quad (2)$$

2.0 Feedback Control Of A Buck Converter SM Power Supply

A typical step-down SM power supply, shown in Figure 1 consists of a buck converter, which is a step-down converter architecture [5-7] and a feedback control system to regulate the output voltage, which must be held within specification during variations in line and load conditions. Negative feedback adjusts the converter duty cycle, D , to maintain the desired output voltage. Duty cycle is typically controlled using a constant pulse frequency and varying pulse width, though other methods exist [8].

Figure 2 shows a buck converter. A flip-flop is used so that Q1 and Q2 are switched ON and OFF in a complementary fashion without overlap. The duty cycle, D , is the fraction of the time that Q1 is on. D controls the ratio of the input voltage to output voltage:

$$V_{OUT} = D \cdot V_{IN} \quad (1)$$

In our proposed design Q1 and Q2 are implemented using silicon carbide power junction field effect transistors (SiC JFETs) [9]. The small signal transfer function of the open loop buck system was first derived by Cuk [5-7]:

where:

- \hat{v}_o is the small signal variations in output voltage,
- \hat{d} is the small signal variation in the switching duty cycle,
- V_O is the static output voltage,
- D is the static switching duty cycle,
- C is the output capacitance,
- L is the output inductance,
- R is the load resistance,
- R_{ON} is the on resistance of the power MOSFET,
- R_C is the equivalent series resistance (ESR) of the output capacitor,
- R_L = series resistance of the inductor.
- s is the Laplace complex frequency operator

Equation (2) takes into account the equivalent series resistance of the output inductor, R_L and the switch on resistance, R_{ON} . The transfer function exhibits a zero and two poles. The zero is due to the filter capacitor and its ESR. Normally, R_{ON} and R_L are both much less than R , and the system is underdamped with complex conjugate poles. The approximate transfer function is:

$$G_d(s) \approx \frac{V_O}{D} \left[\frac{1 + sCR_C}{1 + s \left[\frac{L}{R} + C \cdot R + CR_C \right] + s^2 LC} \right] \quad (3)$$

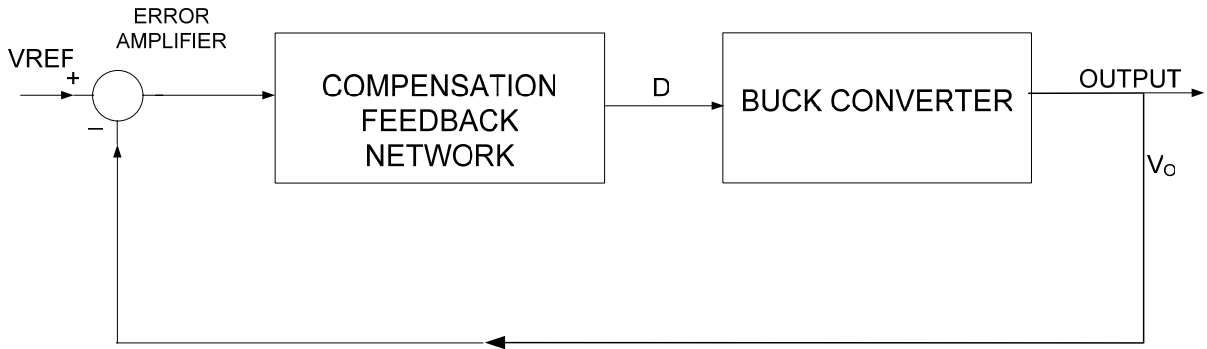


Figure 1. General block diagram of switching regulator or switch mode power supply.

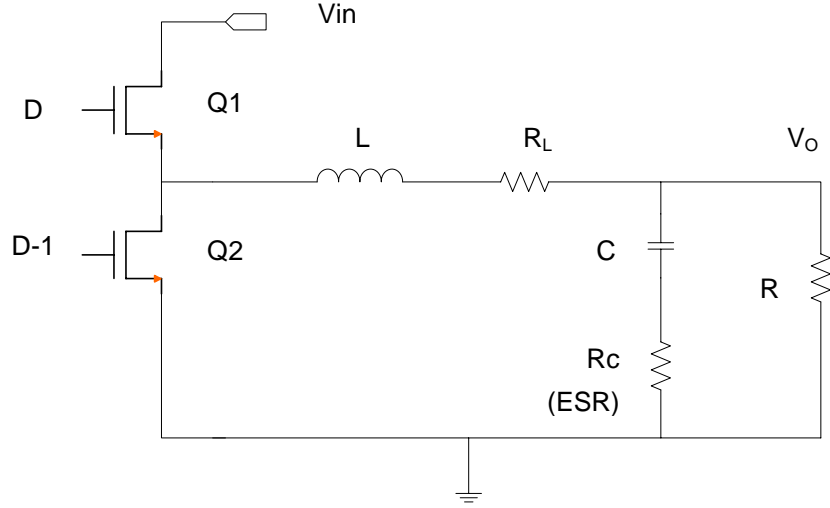


Figure 1. Buck Converter with power switches.

The underdamped response results from the resonance of the inductor and filter capacitor combination. In uncompensated feedback control, the closed loop response of the system will have poor phase margin, and the system will exhibit, ringing, poor settling characteristics, and possible oscillatory instability. This can be ameliorated by properly designed compensation in the feedback network, resulting in a stable, well regulated power supply with good settling characteristics.

The pole and the zero expressions derived from the transfer function of equation (3) are:

$$f_{LC} \approx \pm \frac{i}{2\pi\sqrt{LC}}$$

$$f_{ESR} = \frac{1}{2\pi R_C C} \quad (4)$$

where f_{LC} is the frequency of the complex conjugate poles and f_{ESR} is the zero due to the ESR of the filter capacitor. The current through inductor L is a sawtooth waveform. We define ΔI_L , the inductor ripple current, as the difference between the maximum and minimum periodic inductor current. The ripple current is given by [5,6]:

$$\Delta I_L = \frac{(V_{in} - V_{out}) \times D \times T_{sw}}{2 \times L_{out}} \quad (5)$$

where, T_{sw} is the switching period = $1/f_{clk}$,

The maximum output voltage ripple is defined by the ripple current and the maximum ESR, R_{C-MAX} :

$$\Delta V_{rip} = R_{C-MAX} \Delta I_L \quad (6)$$

The condition for minimum ripple [5,6] occurs when:

$$C \gg \frac{1}{\omega \sqrt{(R^2 - R_C^2)}} \quad (7)$$

Closing the control loop allows the regulator to adjust to line and load perturbations while maintaining output voltage accuracy. A properly designed compensated feedback network will produce a power supply with well defined bandwidth, approximating a overdamped system whose Q approaches 50%.

3.0 V² Architecture

The V² control scheme is attractive for several reasons: 1) it exhibits excellent transient response to both load and line variations, 2) it offers inherent over-voltage protection, and 3) it is easily compensated [1]. A V² controller IC [2, 10] will consist of digital logic, an OTA (operational transconductance amplifier), and two comparators. In this section the operation of the V² control architecture and a design strategy in developing SM power supplies employing V² control is outlined.

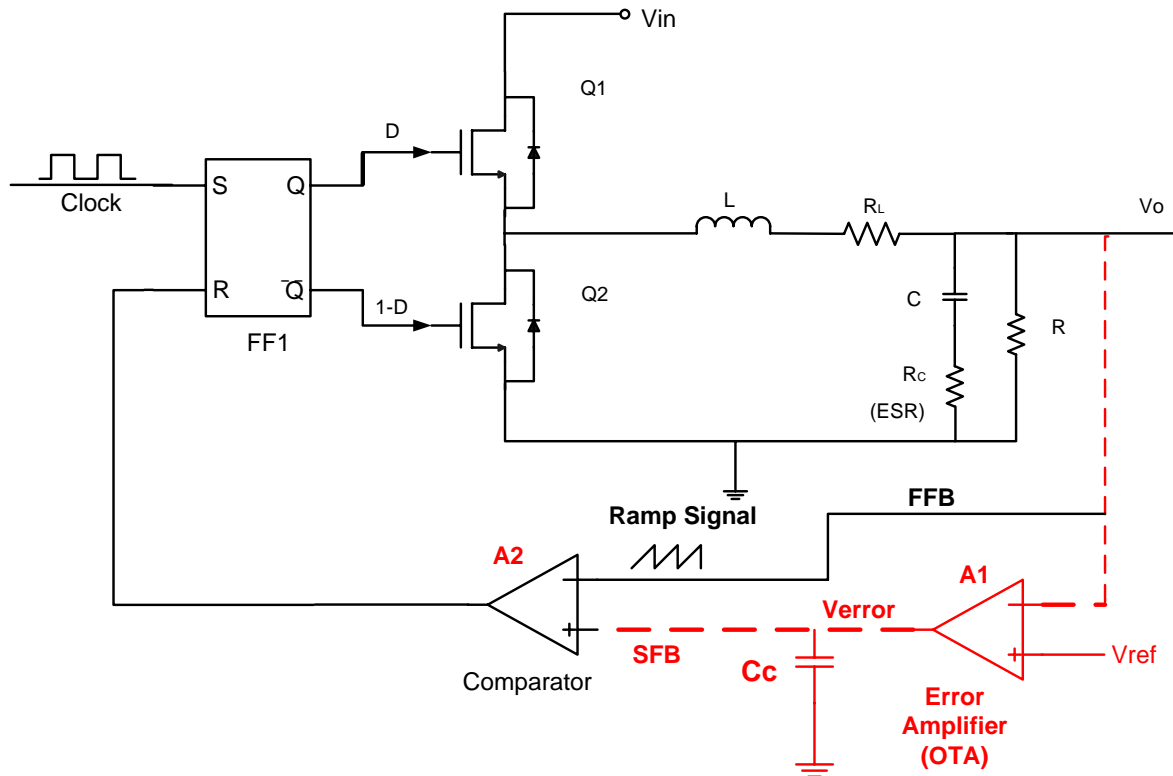


Figure 3. Block diagram of V^2 control scheme with fast feedback path and slow feedback path (dashed line).

Figure 3 shows a diagram of a buck converter with V^2 mode control. FET switches Q_1 and Q_2 , together with inductor L and filter capacitor C are the output inductor and output filter capacitor forming the buck converter. Set-reset flipflop FF1 is driven at the switching frequency and provides complementary control signals to Q_1 and Q_2 , so that when Q_1 is on, Q_2 is off and vice versa. Error amplifier A1 provides a low frequency signal proportional to the difference between the output voltage, V_o , and the desired output voltage, V_{ref} . This error signal is applied to high speed comparator A2. The other terminal of A2 is connected directly to the output voltage which has a small high frequency sawtooth component caused by the inductor ripple current falling across the ESR of the filter capacitor. Each switching cycle, the rising edge of the clock sets FF1, turning off Q_2 , and turning on Q_1 , connecting V_{in} to inductor L . The current in L increases linearly with slope $(V_o - V_{in})/L$. The rising inductor current falls across the filter capacitor ESR, causing an increase in output voltage V_o . When this voltage exceeds the error signal V_{error} on the non-inverting input of comparator A2, A2 switches state and resets flip-flop FF1. Flip-flop FF1, turns off Q_1 , disconnecting inductor L from V_{in} , and turns on Q_2 ,

connecting L to ground. The inductor current ramps down linearly with slope $-V_o/L$, and the voltage across the filter capacitor ESR drops. The output voltage drops until the rising edge of the next input clock pulse, when FF1 is set again and the cycle repeats.

The duty cycle, D , is the fraction of the time that Q_1 is turned on during each clock cycle. Operationally, A1 adjusts the error voltage V_{error} so that its magnitude relative to output voltage with ramp signal will produce duty cycle D that keeps the output voltage equal to the reference voltage. For on-chip implementations the maximum voltage at the input of the amplifier is subject to its input common mode range (ICMR) limitations.

The controller utilizes a slow error signal through error amplifier A1, and a fast path direct signal from V_o . As a result any changes in the load current causes an immediate output change which shows up at the comparator input as a ramp shift. Similarly, any changes in the line voltage changes the current through the inductor, which again appears as a ramp voltage change. As a result all load and line perturbations show up immediately at the input of the comparator, allowing V^2 control to immediately compensate. Practically, V^2 control response is

limited by the combined delay of: 1) the comparator, 2) the control logic, 3) the power switches, and 4) the inductor. From Figure 3 there are two paths from the voltage output to the comparator. The resulting transfer function of the feedback network is [1]:

$$H(s) = FM(1 + A(s))$$

$$H(s) = A_{vol} \cdot FM \left(\frac{1 + \frac{s}{g_m/C_c}}{1 + \frac{s}{g_o/C_c}} \right) \quad (8)$$

where $FM = \frac{2L}{(V_g - V_o) \cdot R_c \cdot T_{sw}}$ serves the role of unit conversion from volts to duty cycle and g_m and g_o are the forward and output transconductance of the compensation OTA. The open and closed loop transfer functions are:

$$H_{open}(s) = \frac{V_o}{D} A_{Vol} \cdot FM \left[\frac{\frac{1}{LC} (1 + sCR_c)}{\frac{1}{LC} + s \left[\frac{R_c}{L} \right] + s^2} \right] \cdot \left[\frac{1 + \frac{s}{g_m/C_c}}{1 + \frac{s}{g_o/C_c}} \right] \quad (9)$$

$$H_{cl}(s) = \frac{H_{open}(s)}{1 + H_{open}(s)} \quad (10)$$

From (9) and (10) the key design observations are made; a) at “DC” the closed loop error or accuracy is inversely proportional to A_{Vol} of the compensation OTA, b) g_m/C_c must be selected less than f_{LC} , c) Q equals $R_c \sqrt{C/L}$ determines the phase margin and settling time, with the resulting requirement, $f_{ESR}/f_{LC} \approx 2-5$, d) the GBP of the closed loop system must be less than $A_{Vol} \times f_{ESR}$, and e) the logic delay must be $\ll 1/(A_{Vol} \times f_{ESR})$.

For a discussion of V^2 controller design, assume that we’d like to build a high temperature power supply using a CMOS-SOS controller with the following typical target specifications: input voltage; 25V, output voltage; 5V, output power; 3W, ripple current; 20% of the output current, and output voltage accuracy; 2% of output voltage. The design flow, depicted in Figure 4, has multiple trade-offs related to processes or device performance, including: the inductor size, switching frequency,

voltage ripple, filter capacitor size and filter capacitor ESR. The selected processes (logic, comparator, and power switches) set an upper bound on the switching frequency, $f_{clk-max}$. An initial clock frequency is selected as $f_{clk-max}/3$ at the highest anticipated operating temperature of the SOS CMOS process.

Design flow is summarized in the following steps. The selected switching frequency, f_{clk} , in conjunction with Equation (5) determines minimum inductance L_{min} . Maximum R_c and minimum C are determined using Equation (6) and Equation (7) respectively. The desired phase margin, PM, or Q of the buck converter response is used to calculate C . The lower bound for A_{vol} of the error OTA is determined by the required DC accuracy, while g_m/C_c is determined by the constraint that g_m/C_c be less than approximately $0.1/\sqrt{LC}$. This design sequence should be followed by analysis and later simulations to ensure adequate PM, current ripple, and voltage ripple and design adjustments are made as necessary.

Assuming the design specification outlined above, with an SOS CMOS controller IC, SiC power switches, a 225 °C working temperature and the topology of Figure 5, several observations are made: 1) $f_{clk-max}$ will be set by the delay of the SiC power switches, 2) a 225 °C inductor L can be implemented while the lack of high capacity high temperature capacitors will severely limit the selection of C , and 3) the OTA, comparators and voltage reference are readily implemented in SOS CMOS and will be summarized following the SPICE simulation results.

4.0 V^2 Architecture SPICE Simulations

The block diagram of a proposed V^2 SOS CMOS IC summarized in Figure 1 is combined with the buck converter of Figure 2 where the specifications of L , C , C_c , the error OTA, and comparator, are derived via the design flow of Figure 4. We omit discussions and SPICE simulations of undervoltage, protection, overvoltage protection, overcurrent protection, and soft start.

All logic, comparators, and OTAs, used in simulations are based on SOS CMOS macro-models or the models taken from Oklahoma State University’s high temperature SOS cell library[11]. The switching frequency is 150 KHz, assumed operating temperature range from 25 °C to 225°C, and values of L , C , and OTA g_m of 225 uH, 300 uF and 5 mS respectively were used.

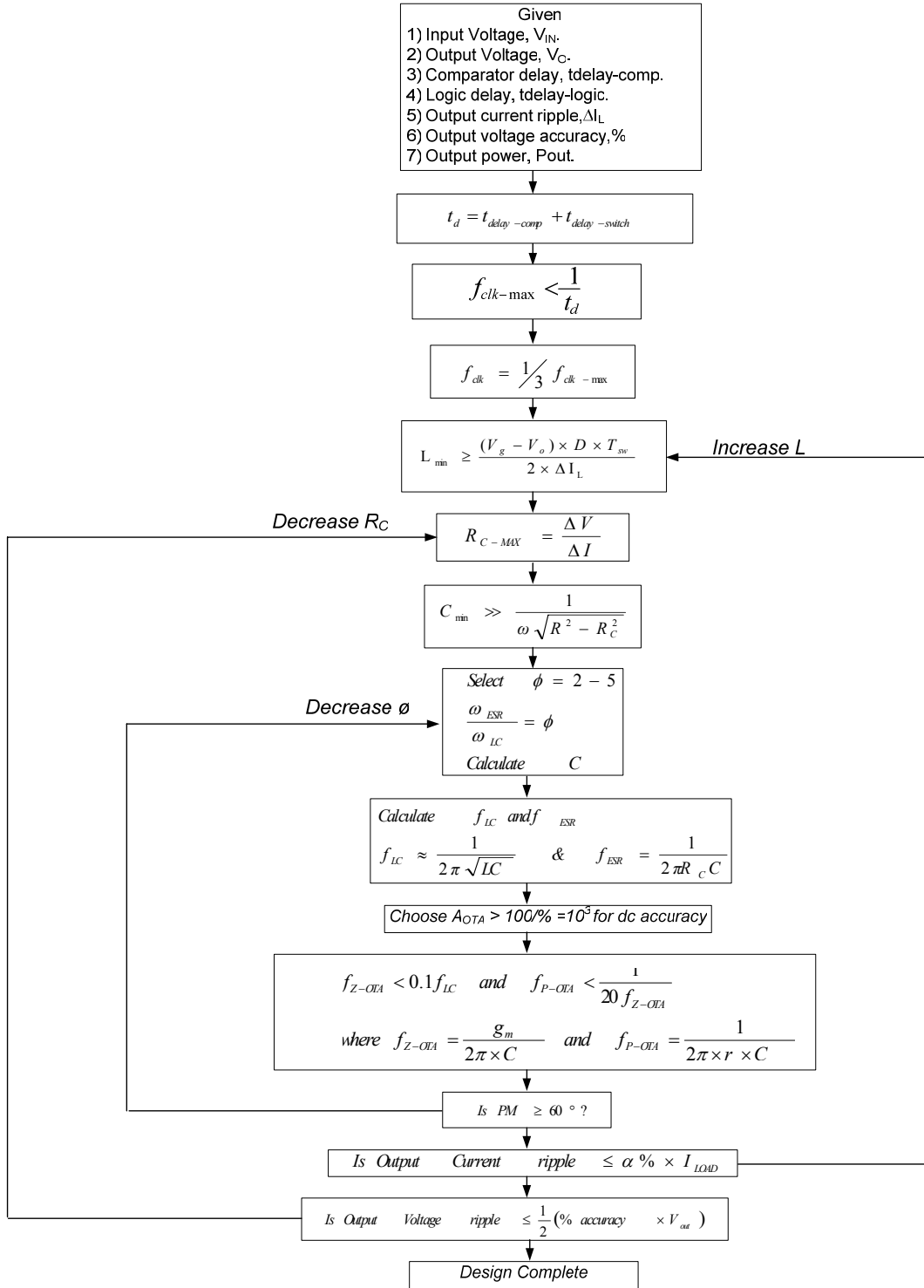


Figure 4 V² design flow algorithm.

The simulation results demonstrate the feasibility of an extreme temperature switched-mode power supply employing V² control. The closed loop output of the power supply holds regulation while the load was varied from 8.33 ohm to 4.165 ohm and

back to 8.33 ohm while individual key components were varied. To investigate robustness of design as a function of the uncertainty of component values, C and L were kept within ± 50% of their nominal values, and g_m , of the error OTA, nominally 5 mS,

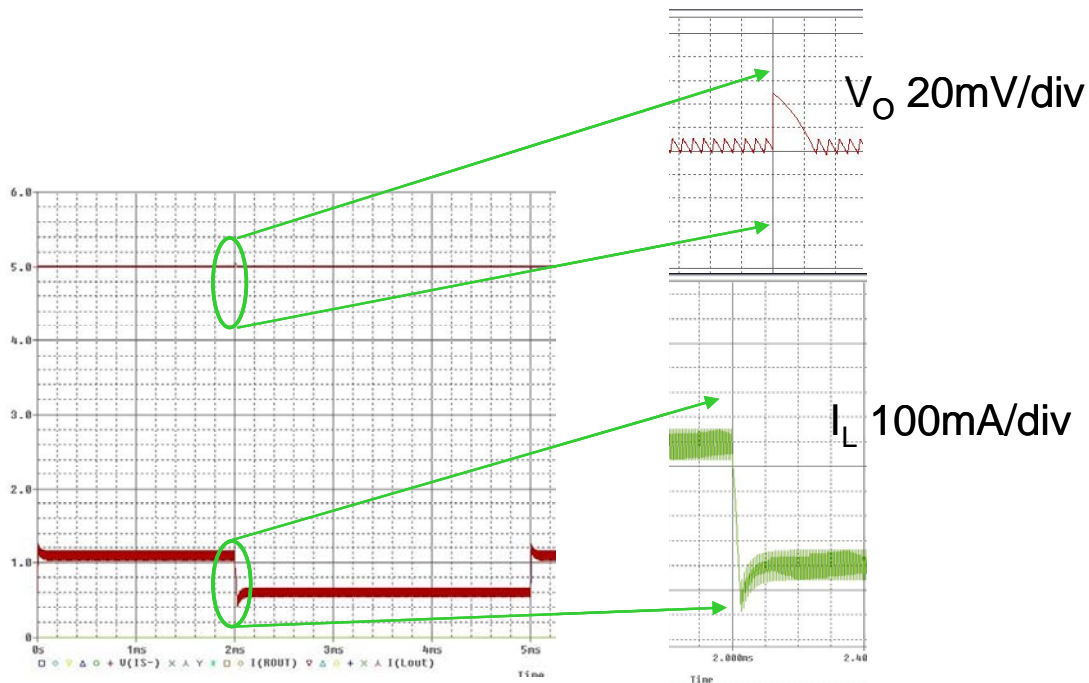


Figure 6. Plots of V_O and I_O as C , the Buck capacitance, is swept from 150 μ F to 450 μ F in 60 μ F steps, validating regulation as the load is varied from full load to 54% load and back to full load. V_O and I_L units are 1V and 1A per major division.

a successful design in SOS CMOS if L and C can be pre selected at assembly time. The SM supply employing V^2 control topology is operational from room temperature to 225°C. The design methodology presented here proves to be an excellent approach to designing both the V^2 SM converter and the V^2 controller IC over a wide range of performance specifications.

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